

**REMARKS**

Claims 13 and 28-30 have been amended and claims 37-39 have been added. Claims 1-39 are pending in the application. Reconsideration of the application is requested in view of the amendments and the remarks to follow.

New claims 37-39 are supported at least by text appearing at page 8, line 11 through page 14, line 3 of the application as originally filed. No new matter is added by new claims 37-39. New claims 37-39 are similar to claims 5-8 but differ in scope. New claims 37-39 distinguish over the art of record and are allowable.

Claims 13 and 28-30 have been amended to correct minor informalities and to respond to the concerns noted in the Office Action (page 2), however, these amendments are not intended to alter the scope of the claims.

**Allowable Subject Matter:**

The Office Action is silent with respect to claims 3, 9, 14, 17, 21, 27, 31 and 34, other than description relative to claim 3 on page 4 and a blanket statement on page 5 to the effect that "Claims 5-26 are rejected on the same ground [sic] as stated above." This still leaves the status of at least claims 27, 31 and 34 with no grounds for rejection and also provides Applicant with no capability for meaningful response with respect to any of claims 5-36. Inasmuch as no meaningful basis for rejection is provided in the Office Action, Applicant assumes that claims 3, 9, 14, 17, 21, 27, 31 and 34 are allowable over the art of record. In the event that the Examiner finds such claims to be not allowable, a subsequent non-final Office Action should be made with such new grounds of rejection.

**Rejection Under 35 U.S.C. §112:**

Claims 13, 28-30 and 32 stand rejected under 35 U.S.C. 35 U.S.C. §112, second paragraph, as being indefinite. Claims 13 and 28-30 have been amended to obviate the concerns noted in the Office Action.

The Office Action states (page 2) that "Claim 32 appears to be a run-on sentence. Appropriate correction is required." Applicant is unable to discern the nature of the issue being explored with respect to claim 32. Clarification of the rejection is requested.

**Rejection under 35 U.S.C. §103:**

The Office Action states (page 3) that claims 1, 2, 4-8, 10-13, 15, 16, 18-20, 22-26, 28-30, 32, 33, 35 and 36 stand rejected under 35 U.S.C. 35 U.S.C. §103(a) over Watson et al., U.S. Patent No. 5,655,132 (hereinafter "Watson"), in view of Applicant's admitted prior art. Applicant respectfully submits that claims 1, 2, 4-8, 10-13, 15, 16, 18-20, 22-26, 28-30, 32, 33, 35 and 36 are not unpatentable over Watson or any admitted prior art and requests reconsideration.

Watson is directed to (Title) a system using a "Register file with multi-tasking support". Watson discloses (Abstract) that "A register file connected to a data memory and an arithmetic logic unit for temporary storage of operands, and a method of managing such register file permits the register file to be used to maximum efficiency, and permits rapid task and context switching. Each register of the register file has an absolute address. A relative register address is read from the address field of the instruction being executed by the ALU, and an arithmetic calculation is performed on that relative register address and a register base address to obtain an absolute register address of the register to be accessed. Different sets of registers may be designated for different tasks or contexts. Each set of registers has its own base address. Once the task or context to which the instruction applies is determined, a calculation using the relative address from the instruction address field, and the corresponding register set base address may be performed to obtain the absolute address of the register to be accessed. Registers assigned to a different task or context may be virtually immediately accessed, or a set of registers for a particular task or context may be moved within the register

file without affecting the instructions being executed by the ALU, by simply changing the base address used in the address computation."

The Office Action states (page 3, item 6) that "Regarding claim 1, Watson discloses in a computer device having a processor that generates a first address signal of a first width and a second address signal of a second width that is greater than the first width (col. 10, lines 13-21, 44-59, fig. 5) ...."

Watson is silent regarding generation of address signals, as recited within claim 1. The passage in col. 10, lines 10-21 of Watson is reproduced below:

A call instruction may contain a displacement field (RFD), which is used to modify the subset base register address RFB to relocate the register file window or subset. The new subset base register address may be calculated by adding to the old base register absolute address the displacement RFD+2. Thus:

$$\text{New RFB} = \text{Old RFB} + \text{RFD} + 2$$

The two is added to the displacement to automatically protect the return information in the local registers LRO and LR1.

Adding a displacement value, as described in this passage, has no effect on address width. Address widths are measured as a number of bits comprising the address. Address width issues are described in Applicant's specification at least at page 2, line 1 et seq.

The passage in Watson at col. 10, lines 38-59 is reproduced below:

When the ALU encounters an exception, or a trap instruction is executed, the register file reserve modifier RFR is used to modify the subset base register address RFB to relocate the register file window. The reserve value RFR is added to the local subset window base address RFB in setting the new subset base address, to move the local window past the registers being protected. The new base register absolute address is calculated from the old base register address by adding the value of the reserve displacement RFR plus two.

Thus:

$\text{New RFB} = \text{Old RFB} + \text{RFR} + 2$

The old RFR value and the return address for the program counter are stored in the new LRO. The status register is stored in the new LR1. A return instruction executed by the ALU restores the local subset window register address RFB to its previous value by subtracting the displacement RFD+2 from it (if a call return), or the register file reserve value RFR+2, if the return is from an exception or trap. In either of these cases, the reserve value, program counter, and status register (if an exception or trap return) are restored.

These passages are void of the teachings for which they are quoted.

Watson is silent regarding generation of address signals for peripheral devices, as recited in each of Applicant's independent claims 1, 5, 8, 12, 16, 20, 24 and 33.

Applicant further notes that Watson is void of any mention of any "thread", as recited in each of Applicant's independent claims 1, 5, 8, 12, 16, 20, 24 and 33. Applicant additionally notes that Watson is void of the phrase "operating system", as recited in Applicant's independent claims 1, 12, 20, 24 and 33.

As a result, it is inconceivable that Watson could teach, disclose, suggest or motivate "concurrently executing threads of a plurality of application programs, wherein different ones of the threads indicate one or more address extensions to an operating system", as recited in claim 1 or as alleged in the Office Action (page 3).

Watson is concerned with rapid addressing in a reduced instruction set computing environment (col. 1, line 6 et seq.). In such an environment, Watson teaches (col. 1, line 30 et seq.) that "Access to a register file is faster than access to main memory partially because the register file has fewer storage locations than the main memory unit. Thus, the addressing mechanism reads and decodes a much shorter address than would be required to address the main memory unit."

This is a completely different area of endeavor than that contemplated by Applicant. Further, attempting to modify the teachings of Watson to attempt to arrive at the subject matter of any of Applicant's claims renders the teachings of Watson unsuitable for their intended purpose. For example, Applicant's claim 1 recites "a processor that generates a first address signal of a first width and one or more peripheral devices that are addressed with a second address signal of a second width that is greater than the first width ...."

The teachings of Watson are rendered unsuitable for their intended purpose in adapting the teachings of Watson to attempt to arrive at the subject matter of any of Applicant's claims encompassing peripheral device addressing. Modification of the teachings of Watson to address busses having widths greater than a processor word size, as recited by Applicant, increases the width of the address.

Watson is concerned with decreasing memory access times by using decreased address widths to address a set of registers, rather than main memory, and does not even contemplate addressing peripheral devices. Watson, in fact, is void of the term "peripheral" and cannot provide teachings relative to address schemata for peripheral devices.

It is improper to employ a reference in a manner that renders the teachings of the reference unsuitable for their intended purpose, as is explained below in more detail with reference to MPEP §2143.01 entitled "Suggestion or Motivation To Modify the References". This MPEP section states, in a subsection entitled "THE PROPOSED MODIFICATION CANNOT RENDER THE PRIOR ART UNSATISFACTORY FOR ITS INTENDED PURPOSE", that "If proposed

modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)".

Additionally, the Office Action states that "it would have been obvious ...." to modify the teachings of Watson. However, this unsupported conclusion does not reflect the test for unpatentability.

With respect to all such allegations, as there is no basis for the Examiner's contentions within the cited reference, the only possible motivation for these contentions is hindsight reconstruction wherein the Examiner is utilizing Applicant's own disclosure to construct a reason for modifying the cited reference. The Examiner is reminded that hindsight reconstruction is not an appropriate basis for a §103 rejection. (*See, e.g., Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990) (explaining that hindsight reconstruction is an improper basis for rejection of a claim).) Such an ad hoc conclusion also fails to provide evidence of motivation or suggestion to modify (*see In re Dembiczak*, *infra*).

Further, there is no basis for the Examiner's contentions within the cited reference. No motivation is identified in the reference for the proposed modification and additions to the disclosure of the reference. Moreover, no evidence to motivate modification of the reference is identified. Against this backdrop, the rejection clearly employs an improper 'obvious to try' standard for finding unpatentability (discussed *infra*).

Applicant notes the requirements of MPEP §2143, entitled "Basic Requirements of a Prima Facie Case of Obviousness" (see also MPEP §706.02(j), entitled "Contents of a 35 U.S.C. 103 Rejection."). MPEP §2143 states that "To establish a prima facie case of obviousness, three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." Inasmuch as the reference fails to teach or disclose the elements recited in the claims, the reference cannot provide motivation to modify their teachings to arrive at the invention as claimed, and the Examiner has identified no such teaching or disclosure in the reference. As a result, the first prong of the test cannot be met.

MPEP §2143 further states that "Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

Inasmuch as the reference fails to provide all of the features recited in Applicant's claims, the third prong of the test is not met. As a result, there cannot be a reasonable expectation of success. As such, the second prong of the test cannot be met.

MPEP §2143 additionally states that "The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)." This fourth criterion cannot be met because the reference fails to teach or disclose the elements recited in the claim.

In fact, Watson is directed solely to reducing memory access times in a multitasking RISC computing context. The claimed subject matter addresses a broader range of issues including accession of peripheral devices. There is no motivation or suggestion in Watson to even consider the problems addressed by the instant disclosure, and no guidance whatsoever to point the artisan towards the claimed subject matter.

No guidance has been identified within the reference to determine which elements to pick or choose from the reference, or of how to couple them to somehow arrive at subject matter such as is claimed. Accordingly, the unpatentability rejections fail all of the criteria for establishing a prima facie case of obviousness as set forth in the MPEP.

There is no teaching or guidance identified within Watson to aid one of ordinary skill in picking and choosing elements from the diverse embodiments of Watson or in assembling those elements to attempt to arrive at the subject matter of any of Applicant's claims. As such, the rejection employs an improper "obvious to try" standard of unpatentability.

Such is improper, as is discussed below in more detail with reference to MPEP §2145(X)(B), entitled "Obvious To Try Rationale". This MPEP section states that "The admonition that 'obvious to try' is not the standard under §103 has been directed mainly at two kinds of error. In some cases, what would have been 'obvious to try' would have been to vary all parameters or try each of numerous possible choices until one possibly arrived at a successful result, where the prior art gave either no indication of which parameters were critical or no direction as to which of many possible choices is likely to be successful. In others, what was

'obvious to try' was to explore a new technology or general approach that seemed to be a promising field of experimentation, where the prior art gave only general guidance as to the particular form of the claimed invention or how to achieve it." *In re O'Farrell*, 853 F.2d 894, 903, 7 USPQ2d 1673, 1681 (Fed. Cir. 1988) (citations omitted)".

In this instance, no guidance in selecting some but not others of the elements described within the teachings of Watson is identified. Similarly, no direction as to which of many possible choices is likely to be successful has been identified.

As there is no basis for the Examiner's contentions within the cited references, the only possible motivation for these contentions is hindsight reconstruction wherein the Examiner is utilizing Applicant's own disclosure to construct a reason for combining and/or modifying the teachings of the cited references. The Examiner is reminded that hindsight reconstruction is not an appropriate basis for a §103 rejection. (See, e.g., *Interconnect Planning Corp. v. Feil*, 227 USPQ 543, 551 (Fed. Cir. 1985); *In re Mills*, 16 USPQ2d 1430 (Fed. Cir. 1990) (explaining that hindsight reconstruction is an improper basis for rejection of a claim).)

Moreover, with respect to all of the unpatentability rejections, no evidence has been provided as to why it would be obvious to modify the teachings of the reference. Evidence of a suggestion to combine or modify may flow (i) from the prior art reference itself, (ii) from the knowledge of one skilled in the art or (iii) from the nature of the problem to be solved. However, this range of sources does

not diminish the requirement for actual evidence. Further, the showing must be clear and particular. See *In re Dembiczak*, 175 F.3d 994, 998 (Fed. Cir. 1999).

For at least these reasons, Applicant respectfully requests that the §103 rejections be withdrawn, and that Applicant's claims 1-36 be allowed.

**Conclusion**

Claims 1-39 are in condition for allowance. Applicant respectfully requests reconsideration and issuance of the subject application. Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

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